REMARKS

This amendment responds to the Office Action dated November 5, 2002 in which the Examiner objected to claim 12, rejected claims 1-4, 6-8, 13, 14 and 17 under 35 U.S.C. §103 and objected to claims 5, 9-12, 15, 16 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

As indicated above, the claims have been amended in order to make explicit what is implicit in the claims. The amendments are unrelated to a statutory requirement for patentability and do not narrow the literal scope of the claims.

Claim 1 claims a semiconductor device comprising a gate electrode, first and second diffused layers, a wiring layer and a contact. The gate electrode is formed on a substrate through a gate insulating film lying therebetween. The first and second diffused layers are formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type. Each layer has a second conduction type different from the first conduction type of the substrate portion. The wiring layer is formed above the gate electrode. The contact is formed within a contact hole between the wiring layer and the substrate. The contact electrically connects the wiring layer to the first diffused layer and a side wall of the gate electrode.

Through the structure of the claimed invention having a contact electrically connecting a wiring layer to the first diffused layer and the side wall of the gate electrode, as claimed in claim 1, the claimed invention provides a semiconductor device which has an improved soft error resistance. The prior art does not show, teach or suggest a contact

electrically connecting a wiring layer to a side wall of the gate electrode as claimed in claim 1.

Claim 4 claims a semiconductor device comprising a gate electrode, a diffused layer, a wiring layer and a contact. The gate electrode is formed on a substrate through a gate insulating film. The diffused layer is formed on the substrate. The wiring layer is formed above the gate electrode. The contact is formed within a contact hole between the wiring layer and substrate. The contact electrically connects the wiring layer to the diffused layers and a side wall of the gate electrode. The diffused layer has first and second portions formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type. Each of the first and second portions has a second conduction type different from the first conduction type of the portion of the substrate. A third portion connects the first portion to the second portion.

Through the structure of the claimed invention having a contact electrically connecting the wiring layer to both the diffused layer and a side wall of the gate electrode, as claimed in claim 4, the claimed invention provides a semiconductor device with an improved soft error resistance. The prior art does not show, teach or suggest a contact electrically connecting a wiring layer to a side wall of gate electrode as claimed in claim 4.

Claims 1-4, 6-8, 13, 14 and 17 were rejected under 35 U.S.C. § 103 as being unpatentable over *Igarashi et al.* (U.S. Patent No. 6,299,314) in view of prior art Figure 31.

Igarashi et al. appears to disclose in Figure 20, MOS transistors Q5 and Q6, each being isolated by a STI film ST, are disposed on a silicon substrate 1. A gate structure

GT64 is disposed as a gate wiring, on the STI film ST. The MOS transistors Q5 and Q6 have gate structures GT65 and GT66, respectively, and a source/drain layer 7 disposed in the surface of the silicon substrate 1 lying on both sides of the gate structures GT65 and GT66. A salicide layer 61 formed from cobalt salicide is disposed on the surface of the source/drain layer 7. The gate structure GT64 comprises a gate oxide film 2 on the STI film ST, gate electrode 3 which is formed from polysilicon and disposed on the gate oxide film 2, an upper nitride film 4 on the gate electrode 3, and a sidewall nitride film 5 disposed such as to make contact with the side faces of the upper nitride film 4, gate electrode 3 and gate oxide film 2. The gate structure GT65 comprises a gate oxide film 2 on the silicon substrate 1, a gate electrode 3 which is formed from polysilicon and disposed on the gate oxide film 2, an upper nitride film 4 on the gate electrode 3, and a sidewall nitride film 5 disposed such as to make contact with the side faces of the upper nitride film 4, gate electrode 3 and gate oxide film 2. The gate structure GT66 comprises a gate oxide film 2 on the silicon substrate 1, a gate electrode 3 which is formed from polysilicon and disposed on the gate oxide film 2, a salicide layer 6 on the gate electrode 3, and a sidewall nitride film 5 disposed such as to make contact with the side faces of the salicide layer 6, gate electrode 3 and gate oxide film 2. An oxide film 8 and nitride film 9 which are disposed such as to follow the contours of the gate structures GT65 and GT66 remain partially on the upper parts of the gate structure s GT65 and GT66. An interlayer insulating film 10 formed from a silicon oxide film is disposed such as to cover the gate structures GT64 to GT66, including the nitride film 9. A contact hole CH12 for exposing the gate structure GT64 penetrates the interlayer insulating film 10 and reaches the

source/drain layers 7 having sandwiched therebetween the STI film ST. A conductor layer CL12 formed from, for example, tungsten is buried in the contact hole CH12, thereby forming the shared contact that connects concurrently the respective source/drain layers 7 of the MOS transistor Q5 and Q6. In the gate structure GT64, since the gate electrode 3 is covered with the nitride film, it can be prevented from being exposed due to the etching of the interlayer insulating film 10, and there is no possibility of being electrically connected to the respective source/drain layers 7 of the gate structures GT65 and GT66. (col. 20, line 55 through col. 21, line 39)

Thus, *Igarashi et al.* merely discloses that the conductor layer CL12 formed in the contact hole CH12 is in contact with a side wall nitride film 5. Thus, nothing in *Igarashi et al.* shows, teaches or suggests that the contact electrically connects the wiring layer to a side wall of the gate electrode as claimed in claims 1 and 4. Rather, *Igarashi et al.* teaches away from the claimed invention since the conductor layer CL12 connects to a side wall nitride film 5.

Figs. 30 and 31 show a well area 10, a diffused layer 20, a gate electrode 30, an interlayer film or dielectric 50, and a common contact hole 60. This common contact hole 60 has a structure in which the gate electrode 30 and the diffused layer 20 corresponding to source/drain are situated at some distance to prevent their overlapping. This is to avoid a problem that the gate electrode 30 and the substrate 10 may be shorted by passing the gate electrode 30 through the thin gate oxide film under the gate electrode when the gate electrode 30 extends onto the silicon substrate. Actually, a sidewall of SiO_2 is provided in an isolation portion between the gate electrode 30 and diffused layer 20 in order to avoid

the short between the gate electrode 30 and the substrate. However, this structure is not illustrated in Figs. 30 and 31 for simplicity.

Thus, prior art Figure 31 merely discloses a side wall of SiO_2 provided between the gate electrode 30 and diffused region 20 as well as a contact hole 60. Thus, nothing in the prior art shows, teaches or suggests a contact electrically connecting a wiring layer to a side wall of the gate electrode as claimed in claims 1 and 4. Rather, the prior art merely discloses that the contact hole 60 is in fact in contact with the unshown sidewall.

The combination of *Igarashi et al.* and prior art Figure 31 would merely suggest a contact which connects to a sidewall of an insulating material. Thus, nothing in the combination shows, teaches or suggests a contact electrically connecting a wiring layer to a side wall of a gate electrode as claimed in claims 1 and 4. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 1 and 4 under 35 U.S.C. § 103 and allows new claim 17.

Claims 2-3, 6-8 and 14 depend from claims 1 and 4 and recite additional features. It is respectfully submitted that claims 2-3, 6-8 and 14 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Igarashi et al.* and prior art Figure 31 at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 2-3, 6-8 and 14 under 35 U.S.C. § 103.

Since objected to claims 5, 9-12, 15 and 16 depend from allowable claims, it is respectfully requested that the Examiner withdraws the objection thereto.

As indicated above, a minor informality in claim 12 has been corrected. It is respectfully requested that the Examiner approves the correction and withdraws the objection thereto.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, Applicants respectfully request the Examiner enters this amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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Marked-up Claims 1, 4, and 12

1. (Amended) A semiconductor device, comprising:

a gate electrode formed on a substrate through a gate insulating film lying therebetween;

first and second diffused layers formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type, each having a second conduction type different from the first conduction type of the portion;

a wiring layer formed above the gate electrode; and

a contact formed within a contact hole between the wiring layer and the substrate, [which connects] the contact electrically connecting the wiring layer to the first diffused layer and a side wall of the gate electrode.

4. (Twice Amended) A semiconductor device, comprising:

a gate electrode formed on a substrate through a gate insulating film;

a diffused layer formed on the substrate;

a wiring layer formed above the gate electrode; and

a contact formed within a contact hole between the wiring layer and the substrate, [which connects] the contact electrically connecting the wiring layer to the diffused layer and a side wall of the gate electrode,

wherein the diffused layer has first and second portions formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type, each having a second conduction type different from the first conduction

Marked-up Claims 1, 4, and 12

type of the portion of the substrate; and a third portion that connects the first portion to the second portion.

12. (Amended) A semiconductor device according to claim 4, comprising a source area and a drain area formed opposed to each other across the channel portion of the substrate existing under the gate electrode, and a transistor for composing a semiconductor IC therein, wherein the impurity concentration of the diffused layer is higher than the impurity concentration [s] of the source area and the drain area.